Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

1.(Currently Amended) A method of forming a split gate field effect transistor, comprising:

providing a substrate having a pair of floating gate layer portions, a first conductive material layer between said pair of floating gate layer portions, and a first dielectric layer above said first conductive material layer;

forming a pair of floating gates from said pair of floating gate layer portions using the first dielectric layer as a first etching hard mask;

forming a substantially rectangular control gate having a second dielectric layer above said control gate, wherein said control gate is self-aligned to said pair of floating gates by using said first and second dielectric layers as a second etching hard mask, said control gate not overlaying said pair of floating gates;

forming a pair of source/drain regions into said substrate and beside said pair of floating gates and said control gate.

2.(Original) The method of claim 1, wherein each of said first dielectric layer and said second dielectric layer comprises a silicon oxide layer.

3.(Original) The method of claim 2, wherein said second dielectric layer is formed by a method of thermal oxidation.

4.(Original) The method of claim 2, wherein said silicon oxide layer has a thickness from about 50 angstroms to about 400 angstroms.

5.(Original) The method of claim 1, wherein said second dielectric layer is thicker at a middle portion than at an edge portion.

6.(Previously Presented) The method of claim 1, wherein said step of forming said control gate comprises:

forming a second conductive material layer above said substrate;

forming a hard mask layer above said second conductive material layer;

removing portions of said hard mask layer and said second conductive material layer;

forming said second dielectric layer above said second conductive material layer; and

removing a remaining portion of said hard mask layer and an additional portion of said second conductive material layer by using said first dielectric layer and said second dielectric layer as said second etching hard mask.

7.(Original) The method of claim 6, wherein said second dielectric layer is formed by using said hard mask layer as an oxidation resistant layer.

8.(Original) The method of claim 7, wherein said hard mask layer comprises a silicon nitride layer.

9.(Previously Presented) The method of claim 6, wherein said step of removing portions of said hard mask layer and said second conductive material layer comprises:

forming a sacrificial layer above said hard mask layer;

removing portions of said sacrificial layer, said hard mask layer and said second conductive material layer;

removing a remaining portion of said sacrificial layer.

10.(Original) The method of claim 9, wherein said sacrificial layer is used to planarize a surface of said substrate.

11.(Original) The method of claim 10, wherein said sacrificial layer comprises an organic material layer.

12.(Original) The method of claim 11, wherein said organic material layer comprises a photoresist.

13.(Original) The method of claim 10, wherein said sacrificial layer comprises a spin-on glass layer.

14-33.(Canceled)

34.(Previously Presented) The method of claim 1, wherein said second dielectric layer is formed by a method of thermal oxidation.

35.(Previously Presented) The method of claim 1, wherein each of said dielectric layers has a thickness from about 50 angstroms to about 400 angstroms.

36.(Currently Amended) A method of forming a split gate field effect transistor, comprising:

providing a substrate comprising a pair of floating gate layer portions and a first conductive material layer between said pair of floating gate layer portions and spaced therefrom;

forming a first dielectric layer above said first conductive material layer;

forming a pair of floating gates from said pair of floating gate layer portions using the first dielectric layer as a first etching hard mask;

forming a substantially rectangular control gate comprising a second dielectric layer above said control gate, wherein said control gate is self-aligned to said pair of floating gates by using said first and second dielectric layers as a second etching hard mask, said control gate not overlaying said pair of floating gates.

37.(Previously Presented) The method of claim 36, wherein said step of forming said control gate comprises:

forming a second conductive material layer above said substrate;

forming a hard mask layer above said second conductive material layer;

removing portions of said hard mask layer and said second conductive material layer;

forming said second dielectric layer above said second conductive material layer; and

removing a remaining portion of said hard mask layer and an additional portion of said second conductive material layer by using said first dielectric layer and said second dielectric layer as said second etching hard mask.

38.(Previously Presented) The method of claim 37, wherein said step of removing portions of said hard mask layer and said second conductive material layer comprises:

forming a sacrificial layer above said hard mask layer;

removing portions of said sacrificial layer, said hard mask layer and said second conductive material layer;

removing a remaining portion of said sacrificial layer.

39.(Currently Amended) A method of forming a split gate field effect transistor, comprising:

providing a substrate comprising a pair of floating gates and a first conductive material layer between said pair of floating gate layers and spaced therefrom, and a first dielectric layer above said first conductive material layer;

forming a substantially rectangular control gate comprising a second dielectric layer above said control gate, wherein said control gate is self-aligned to said pair of floating gates by using said first and second dielectric layers as an etching hard mask, said control gate not overlaying said pair of floating gates.

40.(Previously Presented) The method of claim 39, further comprising forming a pair of source/drain regions into said substrate and beside said pair of floating gates and said control gate.